the input interface, the plurality of logic members processing the plurality of input signals;

at least one coupling unit selectively coupling at least one of the plurality of logic members to another of the plurality of logic members a function of at least one of a plurality of configuration signals;

a register unit selectively storing a portion of the processed input signals; and

an output interface for transmitting the processed input signals;

wherein the input interface of at least one of the plurality of computing cells is selectively coupled to the output interface of at least another of the plurality of computing cells; and

a configuration interface for transmitting the plurality of configuration signals to at least some of the plurality of computing cells to configure the at least some of the plurality of computing cells.

16. (New) The massively parallel data processing apparatus according to claim 15, wherein the at least one coupling unit includes a multiplexer.

17. (New) The massively parallel data processing apparatus according to claim 15, further comprising:

a plurality of lines for selectively coupling at least one of the plurality of computing cells to another of the plurality of computing cells.

18. (New) The massively parallel data processing apparatus according to claim 15, further comprising:

a plurality of lines, at least one of the plurality of lines selectively coupling at least one of the plurality of computing cells to an adjacent

one of the plurality of computing cells, at least another of the plurality of lines selectively coupling at least one of the plurality of computing cells to a non-adjacent one of the plurality of computing cells.

19. (New) The massively parallel data processing apparatus according to claim 15, further comprising:

a synchronization circuit providing a plurality of synchronization signals for synchronizing the configuration of the at least some of the plurality of computing cells.

20. (New) The massively parallel data processing apparatus according to claim 19, wherein the synchronization circuit includes at least one of the plurality of computing cells.

21. (New) The massively parallel data processing apparatus according to claim 15, further comprising

a configuration unit coupled to the configuration interface, the configuration unit generating the plurality of configuration signals, the at least some of the plurality of computing cells being configured as a function of the at least one configuration signal during operation of the massively parallel data processing apparatus such that others of the plurality of computing cells not being configured are not haltered or impaired in their operations.

22. (New) The massively parallel data processing apparatus according to claim 21, further comprising:

a configuration memory coupled to the configuration unit adapted to store the plurality of configuration signals.

23. (New) The massively parallel data processing apparatus according to claim 22, wherein the plurality of configuration signals are stored in the form of a plurality of configuration words.

24. (New) The massively parallel data processing apparatus according to claim 23, wherein the configuration unit manages a plurality of configuration programs, at least one of the configuration programs including at least one of the configuration words.

25. (New) The massively parallel data processing apparatus according to claim 21, wherein the configuration unit is controlled as a function of the plurality of synchronization signals.

26. (New) The massively parallel data processing apparatus according to claim 15, further comprising:

a configuration unit coupled to the configuration interface, the configuration unit adapted to dynamically reconfigure the massively parallel data processing apparatus.

27. (New) The massively parallel data processing apparatus according to claim 26, wherein the configuration unit is adapted to dynamically reconfigure the massively parallel data processing apparatus during a program sequence while data is still processed by the massively parallel data processing apparatus.

28. (New) The massively parallel data processing apparatus according to claim 27, wherein said configuration unit is adapted to dynamically reconfigure without influencing the data to be processed.

29. (New) The massively parallel data processing apparatus according to claim 15, wherein the input interface of at least

one of the plurality of computing cells is coupled to an external memory device.

30. (New) The massively parallel data processing apparatus according to claim 15, wherein the input interface of at least one of the plurality of computing cells is coupled to a peripheral device.

31. (New) The massively parallel data processing apparatus according to claim 15, wherein the input interface of at least one of the plurality of computing cells is coupled to at least a second massively parallel data processing apparatus.

32. (New) The massively parallel data processing apparatus according to Claim 15, further comprising:

a plurality of lines, at least one of the plurality of lines selectively coupling at least one of the plurality of computing cells to an adjacent one of the plurality of computing cells, at least another of the plurality of lines selectively coupling at least one of the plurality of computing cells to a non-adjacent one of the plurality of computing cells;

wherein the at least another of the plurality of lines are divided in a plurality of segments, wherein each of the plurality of segments is connected to at least another one of the plurality of segments by a tristate-bus-driver.

33. (New) The massively parallel data processing apparatus according to claim 15, further comprising:

a plurality of lines, at least one of the plurality of lines selectively coupling at least one of the plurality of computing cells to an adjacent one of the plurality of computing cells, at least another of the plurality of lines selectively coupling at least one of the plurality of computing

cells to a non-adjacent one of the plurality of computing cells;

wherein the at least another of the plurality of lines are divided in a plurality of segments, wherein each of the plurality of segments is connected to at least another one of the plurality of segments by a transmission gate.

34. (New) The massively parallel data processing apparatus according to claim 15, further comprising:

a plurality of lines, at least one of the plurality of lines selectively coupling at least one of the plurality of computing cells to an adjacent one of the plurality of computing cells, at least another of the plurality of lines selectively coupling at least one of the plurality of computing cells to a non-adjacent one of the plurality of computing cells;

wherein the said at least another of the plurality of lines are divided in a plurality of segments, wherein each of the plurality of segments is connected to at least another one of the plurality of segments by an electrical switch.

35. (New) A massively parallel data processing apparatus, comprising:

a plurality of computing cells arranged in a multidimensional matrix, each of the plurality of computing cells being configurable and reconfigurable, each of the plurality of computing cells capable of processing a first plurality of data words simultaneously with the processing of a second plurality of data words by others of the plurality of computing cells, wherein each of the plurality of computing cells is configured by a first set of configuration words, and wherein each of the plurality of computing cells is reconfigured by a second set of configuration words; and

a plurality of buses, wherein each of the plurality of computing cells are connectable to at least one of the plurality of computing cells using at least one of the plurality of buses.

36. (New) The massively parallel data processing apparatus of claim 35, wherein each of the plurality of computing cells maintaining a first configuration for a first period of time.

37. (New) The massively parallel data processing apparatus of claim 36, wherein at least some of the plurality of computing cells are capable of detecting a need for a reconfiguration.

38. (New) The massively parallel data processing apparatus of claim 36, further comprising:

at least one memory coupled to the processing apparatus for storing at least one of multiple data and processing results.

39. (New) The massively parallel data processing apparatus of claim 36, further comprising:

at least one interface for transferring data coupled to at least one of an external computer and a memory device.

40. (New) The massively parallel data processing apparatus of claim 36, further comprising:

at least one interface coupled to at least one peripheral device.

41. (New) The massively parallel data processing apparatus of claim 36, further comprising:

an interface structure optimized for coupling a plurality of the massively parallel data processing apparatuses.

42. (New) The massively parallel data processing apparatus of claim 36, further comprising:

a compiler capable of reconfiguring each of the plurality of computing cells independently of others of the plurality of computing cells such that portions of the massively parallel data processing apparatus not being reconfigured are not impaired in their operation.

43. (New) The massively parallel data processing apparatus of claim 42, further comprising:

a memory, coupled to the compiler, for storing the first set of configuration words and the second set of configuration words.

44. (New) The massively parallel data processing apparatus of claim 42, wherein the compiler manages a plurality of configuration programs.

45. (New) The massively parallel data processing apparatus of claim 35, further comprising:

a synchronization circuit providing a plurality of synchronization signals for synchronizing the configuration of the at least some of the plurality of computing cells.

46. (New) The massively parallel data processing apparatus of claim 45 wherein at least one of the plurality of computing cells provides status information to the synchronization circuit.

47. (New) A massively parallel data processing apparatus, comprising:

a programmable logic device, the programmable logic device including a plurality of logic elements arranged in a multidimensional matrix, each of the plurality of logic elements being configurable and reconfigurable, each of the plurality of logic elements capable of processing a first plurality of

binary signals simultaneously with the processing of a second plurality of binary signals by others of the plurality of logic units, wherein each of the plurality of logic elements is configured by a first set of configuration words, and wherein each of the plurality of logic elements is reconfigured by a second set of configuration words, the programmable logic device further comprising a plurality of buses, wherein each of the plurality of logic elements are connectable to at least one of the plurality of logic elements using at least one of the plurality of buses;

at least one memory device coupled to the programmable logic device for storing at least one of i) multiple data to be processed by the programmable logic device, and ii) processing results of the programmable logic device; and

at least one of i) an interface coupled to at least one external computer and ii) a further memory device coupled to the at least one external computer, for transferring at least one of multiple data to be processed by the programmable logic device and processing results of the programmable logic device.

48. (New) The massively parallel data processing apparatus of claim 47, wherein each of the plurality of logic elements maintaining a first configuration for a first period of time.

49. (New) The massively parallel data processing apparatus of claim 48, wherein at least some of the plurality of logic elements are capable of detecting a need for a reconfiguration.

50. (New) The massively parallel data processing apparatus of claim 47, further comprising:

at least one peripheral interface coupled to at least one peripheral device.

51. (New) The massively parallel data processing apparatus of claim 47, further comprising:

an interface structure optimized for coupling a plurality of the massively parallel data processing apparatuses.

52. (New) The massively parallel data processing apparatus of claim 47, further comprising:

a compiler capable of reconfiguring each of the plurality of logic elements independently of others of the plurality of logic elements such that portions of the massively parallel data processing apparatus not being reconfigured are not impaired in their operation.

53. (New) The massively parallel data processing apparatus of claim 52, further comprising:

a memory, coupled to the compiler, for storing the first set of configuration words and the second set of configuration words.

54. (New) The massively parallel data processing apparatus of claim 52, wherein the compiler manages a plurality of configuration programs.

55. (New) The massively parallel data processing apparatus of claim 47, further comprising:

a synchronization circuit providing a plurality of synchronization signals for synchronizing the configuration of the at least some of the plurality of computing cells.

56. (New) The massively parallel data processing apparatus of claim 51 wherein at least one of the plurality of logic

elements provides status information to the synchronization circuit.

57. (New) A data processor, comprising:

cells arranged in a multi-dimensional pattern;

a first compiler for individually accessing and individually configuring at least some of the cells, the first compiler selectively grouping the at least some of the cells with neighboring cells into functional units to perform a first function, the first compiler further selectively regrouping selected ones of the at least some of the cells into different functional units to perform a second function different than the first function while simultaneously others of the at least some of the cells process data.

58. (New) The data processor according to claim 57, wherein the first compiler receives state information from at least one cell in each functional unit and selectively regroups the selected ones of the at least some of the cells as a function of the state information.

59. (New) The data processor according to claim 57, further comprising:

a priority decoder for determining an order for the first compiler to selectively regroup the selected ones of the at least some of the cells.

60. (New) The data processor according to claim 57 wherein the first compiler selectively regroups the selected one of the at least some of the cells by transmitting configuration data to at least one of the at least some of the cells, the at least one of the at least some of the cells reconfiguring to logically coupled to another of the cells as a function of the configuration data.

61. (New) The data processor according to claim 57, further comprising:

second cells arranged in a second multi-dimensional pattern coupled in cascade with the cells.

62. (New) A data processor, comprising:

cells arranged in a multi-dimensional pattern, at least one of the cells being selectively coupled to a first one of the cells to form a first functional unit at a first time, the first functional unit performing a first function, the at least one of the cells capable of being regrouped with a second one of the cells to form a second functional unit at a second time different from the first time, the second functional unit performing a second function different from the first function, the at least one of the cells regrouping as a function of reconfiguration data; and

a first compiler receiving state information regarding the state of the first functional unit and transmitting reconfiguration data to the at least one of the cells as a function of the received state information.

63. (New) The data processor according to claim 62, wherein the first compiler determines a program flow as a function of the state information.

64. (New) The data processor according to claim 62, wherein selected ones of the at least one of the cells reconfigure to perform the respective second function while simultaneously others of the at least some of the cells process data.

65. (New) The data processor according to claim 62, further comprising:

a priority decoder determining an order for the first compiler to transmit the reconfiguration data.

66. (New) The data processor according to claim 62, further comprising:

a segmented bus selectively coupling each of the cells to others of the cells.

67. (New) The data processor according to claim 66, wherein the segmented bus including a first segment and a second segment, the first segment providing communication between a first one of the cells and a second one of the cells, the second segment providing communication between a third one of the cells and a fourth one of the cells.

68. (New) The data processor according to claim 62, further comprising:

second cells arranged in a second multi-dimensional pattern coupled in cascade with the cells.

69. (New) A method for configuring a data processor, the data processor including cells arranged in a multi-dimensional pattern, comprising the steps of:

grouping at least some of the cells into functional units;

processing data by the functional units;

receiving, by a reconfiguration unit, state information regarding at least one of the functional units;

transmitting, by the reconfiguration unit, respective configuration data to the at least one of the functional units as a function of the received state information; and

reconfiguring at least one of the cells in the at least one of the functional units as a function of the respective configuration data while simultaneously other functional units continue processing data.

70. (New) The method according to claim 69, further comprising the step of:

regrouping the at least one of the cells with another of the cells into a different functional unit.

71. (New) The method according to claim 69, wherein the receiving step includes the step of receiving the state information from the at least one of the functional units.

72. (New) A method for configuring a data processor, the data processor including cells arranged in a multi-dimensional pattern, comprising the steps of:

individually configuring at least some of the cells to form functional units;

processing data by at least some of the functional units;

individually reconfiguring at least one cell of at least one of the functional units to form a different functional unit while simultaneously others of the functional units continue processing data.

73. (New) The method according to claim 72, further comprising the steps of:

receiving, by a reconfiguration unit, state information regarding at least one of the functional units;

transmitting, by the reconfiguration unit, reconfiguration data to the at least one cell, wherein the step of reconfiguring includes the step of reconfiguring, by the at least one cell, as a function of the reconfiguration data transmitted by the reconfiguration unit.

74. (New) A method for configuring a data processor, the data processor including cells arranged in a multi-dimensional pattern, comprising the steps of:

grouping at least some of the cells into functional units;

enabling by a state machine the at least some of the cells;

after the enabling step, processing data by the functional units;

receiving, by a reconfiguration unit, state information regarding at least one of the functional units;

transmitting, by the reconfiguration unit, respective configuration data to the at least one of the functional units as a function of the received state information;

disabling by the state machine at least some of the cells of the at least one of the function units while others of the function units are still enabled; and

after the disabling step, reconfiguring at least one of the cells in the at least one of the functional units as a function of the respective configuration data while simultaneously other functional units continue processing data.

75. (New) The method according to claim 74, wherein the enabling step includes the step of:

transmitting by the state machine first synchronization signals to the at least some of the cells.

76. (New) The method according to claim 75, wherein the disabling step includes the step of:

transmitting by the state machine second synchronization signals to the at least some of the cells.

77. (New) A method of processing data within a data processor, the data processor including cells arranged in a multi-dimensional pattern, comprising the steps of:

grouping at least some of the cells into functional units;

enabling by a state machine a transfer of data between a first plurality of the cells depending on the presence of the data and a state of at least some of the cells, the first plurality of the cells being in a READY state for at least one of i) accepting new data, and ii) transmitting a result; and

disabling by a state machine the transfer of the data depending on the presence of the data and the state of at least some of the cells, the at least some of the cells being in a NOT ready state for accepting the new data and for transmitting the results.